Overview

The Peraso W110 chipset is targeted for WiGig® applications and employs the PRS1125 and PRS4001 integrated circuits to implement the necessary IEEE 802.11ad functionality. The W110 chipset implements a complete SuperSpeed USB 3.0 to WiGig® solution. The PRS4001 Low Power WiGig® Baseband incorporates the Analog Front End, BB PHY/MAC, and two RISC CPU cores. The PRS1125 is a single chip direct conversion RF transceiver providing 60 GHz single-ended receiver and transmit antenna interfaces. The chipset is ideal for wireless storage, wireless display, and multi-gigabit mobile wireless applications.

Features

PRS4001 Low Power Baseband

- IEEE 802.11ad compliant
- Fully integrated AFE, PHY and MAC
- Highly flexible, dual CPU soft MAC integrates WiGig® MAC functions
- PHY supports MCS0 to MCS12 (4.62 Gb/s)
- 2 Gb/s link at 10m (MCS8)
- 1 Gb/s at 20m (MCS4)
- 0.8 mm thick, 7mm × 7mm BGA

PRS1125 High Performance WiGig® Radio

- Tx output power: Up to +14 dBm
- Better than -21 dB transmit EVM (16-QAM)
- Receiver noise figure: < 5 dB
- Receiver conversion gain > 70 dB
- Integrated single-ended 60 GHz antenna interfaces
- PLL tunes to all channels of IEEE 802.11ad specifications using integrated XO
- 0.7 mm thick, 7mm × 7mm BGA Package

Application Diagram
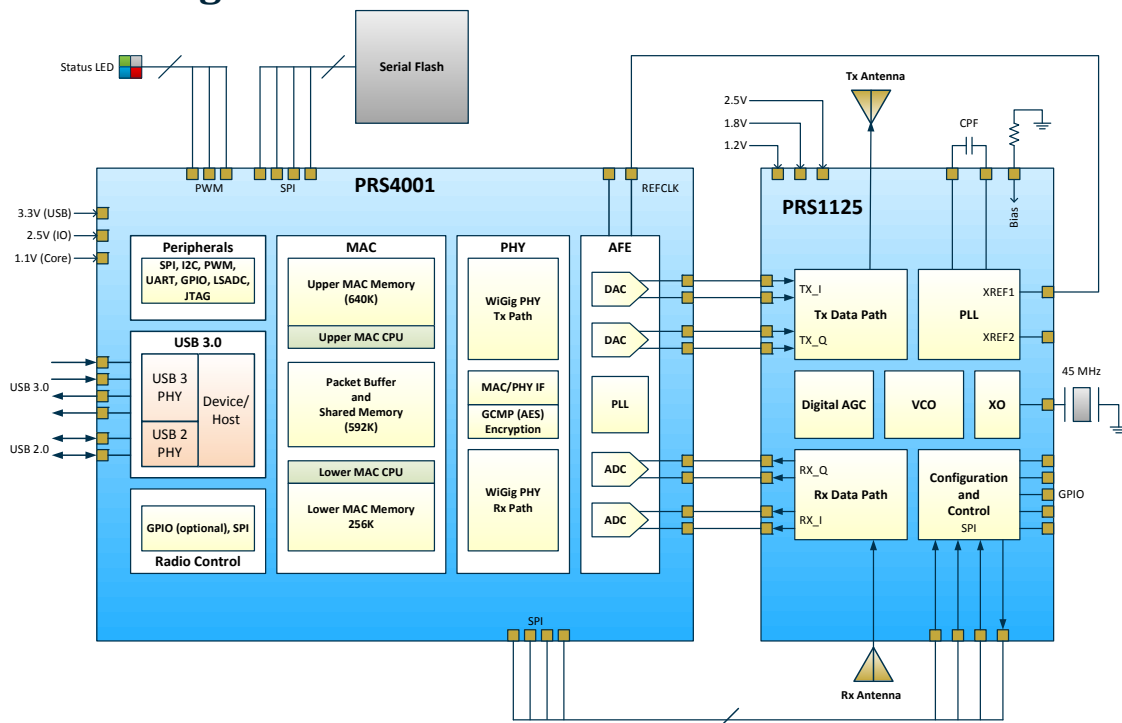
General Description

The Peraso W110 WiGig® chipset is compliant with the single carrier modulation and coding schemes of the IEEE 802.11ad specifications (MSC0 to MSC12). Incorporating the PRS4001 WiGig® baseband IC and the PRS1125 WiGig® radio, the chipset implements a low cost, low power, high performance SuperSpeed USB 3.0 to WiGig® device.

The PRS4001 includes a USB 2.0 and 3.0 device/host system interface. Supporting link speeds in excess of 2.0 Gb/s, it is possible to configure the PRS4001 as a multi-gigabit WiGig® USB adaptor or as the 60 GHz wireless connection for a WSB peripheral device.

The PRS4001 MAC incorporates two powerful RISC processors to provide the highest flexibility in supporting 801.11ad MAC functionality. CPU code boot loading is supported from the USB interface or external serial flash. Security is ensured through the use of AES with a 128-bit key and a 128-bit block size utilizing GCM for data confidentiality and GMAC for authentication and integrity. RSNA and 802.1X are used to provide a robust authentication and association procedure. The MAC includes sufficient internal memory to buffer data transfers to and from the PHY as well as receiving/transmitting packets to the host interfaces. No additional RAM is required.

The PRS4001 PHY is capable of modulating/demodulating all control and single carrier π/2-BPSK, π/2- QPSK and 16-QAM WiGig® coding schemes (MCS0 to MCS12) up to a maximum rate of 4.62 Gb/s. LDPC forward error correction maximizes performance in unreliable or noisy communication channels.

The PRS4001 also includes a highly configurable programmable IO subsystem consisting of GPIO, UART, SPI, TWI, PWM and JTAG. The firmware incorporates multiple layers of debug such logging and extensive statistic and event counters.

The PRS4001 supports seamless connection to all Peraso 60 GHz radios:
- The PRS1025 is a single chip IC incorporating an integrated patch antenna with 8.5 dBi peak gain across the entire 60 GHz band
- The PRS1125 is a single chip RFIC with single-ended 60 GHz Tx and Rx antenna ports
- The PRS2152 and PRS2153 are highly integrated module reference designs with an available WR-15 waveguide interface allowing simple interface to common 60 GHz waveguide components

Applications
- Mobile multi-gigabit wireless connectivity
- Wireless storage devices
- High quality, low latency, wireless UHD 4K display
- Wireless docking stations, I/O and mobile "sync-and-go"
- Small cell backhaul
- Wi-Fi infrastructure and other multi-gigabit links

Standards Compatibility
- IEEE 802.11ad-2012 (WiGig® version 1.3): single carrier modulation and coding schemes
- IEEE 802.11-2012
- IEEE 802.1X-2004
- USB 3.0 Specification, Revision 1.0
- FIPS PUB 197-2001

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